Department of Electronics & Communication Engineering

solicit your benign presence on the occasion of

Valedictory Ceremony

of

Three days' Workshop on

"Analog CMOS Integrated Circuit Design"

(14^{th} -16^{th} April, 2018)

on April 16, 2018 at 12:00Noon

in the Computer Auditorium of the Institute

Prof. Shailendra Jain
Director, SLIET

has kindly consented to be the Chief Guest of the function

and

Prof. M B Bera
Dean (Academics)
&
Er. H S Jatana
Scientist/Engineer 'G" SCL / ISRO, Dept of Space Mohali

will be the Guests of Honour

R.S.V.P

Organizing Committee of the WACICD

Programme Overleaf

INVITATION

Department of Electronics & Communication Engg. is going to organize three days workshop on **Analog CMOS Integrated Circuit Design** for faculty, staff and students of SLIET, Longowal during **14th -16th April, 2018 (Saturday, Sunday & Monday)** as per the details given below:

Venue – Computer Auditorium

Resource Persons: – Er. HS Jatana, Gr Head – Design & Process Group ; Er. Ashutosh Yadav, Sci/Engr 'E' DPG/VDD ; Er. Rajesh Srivastava, Sci/Engr 'D' DPG/VDD

The objective of this workshop is to provide comprehensive coverage of the basic concepts of analog integrated circuits and characteristics. It aims to provide an in-depth knowledge of analog design flow and Device Simulator/ cadence EDA tools.

Schedule

Day 1 (14th April, 2018):

Inauguration	Inauguration at 9:30 AM
LECT01	CMOS Process & Design Challenges in Current Technology
LECT02	Process Integration & Components available in Standard CMOS Technology
LECT03	MOS – Functionality, Models
LECT04	CMOS as a Switch – Issues, Challenges, Problems and remedies
LECT05	CMOS as Amplifier – Issues and Challenges
LAB01	Understanding and Using Device Simulator

Day 2 (15th April, 2018):

LECT06	Single MOS Tx Topologies – CS Configuration (issues in Tx sizes, I/p & O/p swings, lower node issues)
LECT07	CS Configuration – Frequency response. Effect of DSM technology nodes on freq response, effect of Ft and Fmax .
LECT08	Biasing techniques used in Chip Design
LECT09	Concept of Controlled Sources, significance, where, why and how used in chip design
LECT10	VCVS using MOS Tx
LAB02	Analog Design Flow ; Schematic Entry

Day 3 (16th April, 2018):

LECT11	CCCS using MoS Tx – Large signal analysis, Small signal analysis
LECT12	Current sources – relevance and used in chip design
LECT13	Voltage reference – concept, how to use in chip design
LAB03	Layout of Single Tx topology – meaning of DRC,LVS,PEX and its relevance
QUIZ	Brief Quiz of 25 minutes.
Valedictory Ceremony	3:00 PM onwards

terested faculty, staff, research scholars and students are cordially invited to attend the same.

Convener : Dr. Jagpal Singh Ubhi,
rofessor (ECE)

11/4/18

Chairperson : Dr. Anupma Marwaha,
Professor & HOD (ECE)

Copy to:

- Director Cell: for information, please
- All Deans, for information, please
- HODs, with a request to circulate in the respective department

14 - 4 - 2017

DEGREE-2016 (JEE MAIN) & LEET 2017
VLSI workshop

S.NO.	TRADE	REGN NO	NAME OF STUDENTS	SIGNATURE OF STUDENT Morning	Afternoon
1	GEC	1640014	YASHVENDRA CHAUHAN	— X —	X
2	GEC	1640015	RITIKA NEGI	— X —	X
3	GEC	1640019	PULKIT AGGARWAL	— X —	X
4	GEC	1640024	NAVJOT JYOTI	Navjot Jyoti	Navjot Jyoti
5	GEC	1640033	UTTAM KUMAR	— X —	X
6	GEC	1640051	SHUBHAM KUMAR JHA	— X —	X
7	GEC	1640055	SHRISTI PRAKASH	Shristi Prakash	Shristi Prakash
8	GEC	1640056	PANIKAR	— X —	X
9	GEC	1640062	ATISH DEEPANKAR	Atish Deepankar	Atish Deepankar
10	GEC	1640086	RIA SHARMA	Ria Sharma	Ria Sharma
11	GEC	1640090	MUTYALA DEVENDRA VENKAT	—X	X
12	GEC	1640092	ISHPREET KAUR	—X	X
13	GEC	1640103	VARDIREDDY VASUDEVA REDDY	—X	X
14	GEC	1640154	UBAIR ALI	— X	X
15	GEC	1640157	MEHRAJ UD DIN TELI	MEHRAJ - DIN	
16	GEC*	1640034	SUDHANSHU KUMAR	Sudhanshu	Sudhanshu
17	GEC*	1640052	SHEFALI GOYANKA	Shefali Goyanka	Shefali Goyanka
18	GEC	1730964	ASHIF REZA	—X	X
19	GEC	1730981	KUMARI BEENA SINGH	Beena Singh	Beena Singh
20	GEC	1730982	ANJALI SINGH	X	X
21	GEC	1730983	ANSHU VERMA	Anshu Verma	Anshu Verma
22	GEC	1731015	MD SIKANDAR	X	X
23	GEC	1731538	JASLEEN KAUR	X	X
24	GEC	1731561	ANIRUDH GOEL	Aniruddh	Aniruddh
25	GEC	1731562	SHEKHAR KAPUR	Shekhar Kapur	Shekhar Kapur
26	GEC	1731564	AMAN RAJ	X	X
27	GEC	1731565	SHAHANWAZ AHMAD	X	X
28	GEC	1731566	AKANKSHA KUMARI	Akanksha Kumari	Akanksha Kumari
29	GEC	1731567	KESHAV ACHARYA	Keshav Acharya	Keshav Acharya
30	GEC	1731568	PRIKSHIT AWASTHI	X	X

NO. OF STUDENTS PRESENT:..... NO. OF STUDENTS ABSENT: ..... SIGNATURE OF INVIGILATOR: .....

DEGREE-2016 (JEE MAIN) & LEET 2017
VLSI workshop

S.NO.	TRADE	REGN NO	NAME OF STUDENTS	SIGNATURE OF STUDENT Morning	Afternoon
31	GEC	1731569	PRAJJWAL	X	X
32	GEC	1731570	RAVI SHANKAR KUMAR	Ravi Shankar Kumar	
33	GEC	1731571	AMARTYA PAUL	A Paul	A Paul
34	GEC	1731572	BHANU PRATAP AGGARWAL	X	X
35	GEC	1731573	ANAND VERMA	X	X
36	GEC	1731574	NITIN PILLAY	X	X
37	GEC	1731575	DIVYA JYOTI	Divya Jyoti	Divya Jyoti
38	GEC	1731576	BHAWNA PRASHER	X	X
39	GEC	1731577	PRIYA KUMARI	Priya Kumari	Priya Kumari
40	GEC	1731578	SONAM KUMARI	X	X
41	GEC	1731579	PARITOSH CHHABRA	Paritosh	Paritosh
42	GEC	1731580	MANMEET KAUR SAINI	X	X
43	GEC	1731581	AKANKSHA SINGH	Akanksha	Akanksha
44	GEC	1731582	ANU PRIYA BHARTI	Anupriya	Anupriya
45	GEC	1731583	PUSHKAR ANAND	Pushkar Anand	Pushkar Anand
46	GEC	1731584	AMRITA PRITAM	Amrita Pritam	Amrita Pritam
47	GEC	1731585	SACHIN KUMAR	Sachin Kumar	Sachin Kumar
48	GEC	1731586	ISHA KIRTI	Isha Kirti	Isha Kirti
49	GEC	1731587	SHWETA KUMARI	Shweta Kumari	Shweta Kumari
50	GEC	1731588	ARUN BHASKAR	Arun Bhaskar	Arun Bhaskar
51	GEC	1731589	HARSIMRAN KAUR	X	X
52	GEC	1731590	DIVYANSHU RANJAN	Divyanshu Ranjan	Divyanshu Ranjan
53	GEC	1731591	RAUSHAN KUMAR	Raushan Kumar	Raushan Kumar
54	GEC	1731592	SADHANA SHUKLA	Sadhana Shukla	Sadhana Shukla
55	GEC	1731593	PALLAVI RAJ	Pallavi Raj	Pallavi Raj
56	GEC	1731594	NISHU KUMARI	Nishu Kumari	Nishu Kumari
57	GEC	1731596	IRFAN KASMI	X	X
58	GEC	1731597	NEERAJ KUMAR	Neeraj Kumar	Neeraj Kumar
59	GEC	1731598	ROHIT KUMAR	X	X
60	GEC	1731599	MANISH KUMAR	X	X
61	GEC	1731600	SUMIT KUMAR	X	X
62	GEC	1731602	DEV RAJ	Dev raj	Dev raj
63	GEC	1731603	MANISH KUMAR	X	X
64	GEC	1731604	JAYRAM SINGH YADAV	X	X
65	GEC	1731605	SHALINI DHIMAN	X	X
66	GEC	1731606	POOJA PRIYAMBADA	X	X

NO. OF STUDENTS PRESENT:..... NO. OF STUDENTS ABSENT: ..... SIGNATURE OF INVIGILATOR: .....

संत लौंगोवाल अभियांत्रिकी एवं प्रौद्योगिकी संस्थान
Sant Longowal Institute of Engineering and Technology
(Deemed-to-be-University, under MHRD, Govt. of India)

NUMEREGION's TaraNG
Interactive | Learning | Pedagogy

Cloud-based Simulation Practices for Advanced Virtual Labs using myTaraNG

The cloud based interactive simulation solution specially installed for effective blended learning during the pandemic. myTaraNG portal proven to be best fit in current situation

07 TH FEBRUARY 2021 | 6:00 PM

www.mytarang.com

Swapnil Gaul
Founder,
NUMEREGION

Madhura Barshikar
Application Engineer,
NUMEREGION

Coordinators

Dr.Surinder Singh
Head, ECE Department
SLIET Longowal

Dr.Anupma Marwaha
Professor, ECE Department
SLIET Longowal

Mr. Kuldip Singh
Asst. Prof, ECE Dept.
SLITE Longowal

Registration Link: https://forms.gle/hCJKwnu1WkL1wbWv7

Workshop Report

"3 Days workshop on Cloud Based Simulation Practices for Advanced Virtual Labs using My TaraNG "

A three-day online workshop on, "**Cloud Based Simulation Practices for Advanced Virtual Labs using My TaraNG"** has been organized by the department of **Electronics & Communication Engineering** on 07/02/21 onwards with hands on practice sessions covered on 13/02/21 and 14/02/21 respectively for the postgraduate and undergraduate students of the Institute.

The main objective of this workshop was to provide hands on practices about cloud based interactive simulation tool specially installed for effective blended learning to graduate and post graduate students during the pandemic. No financial assistance was taken from the institute and no participation fee was charged from the participants for this workshop.

First day of workshop scheduled on 07/02/2021 covered sign up and sign in process, installation of connector and access of TaraNG simulation software installed on remote system and a demonstration of TaraNG simulation software for designing of different circuits and components.

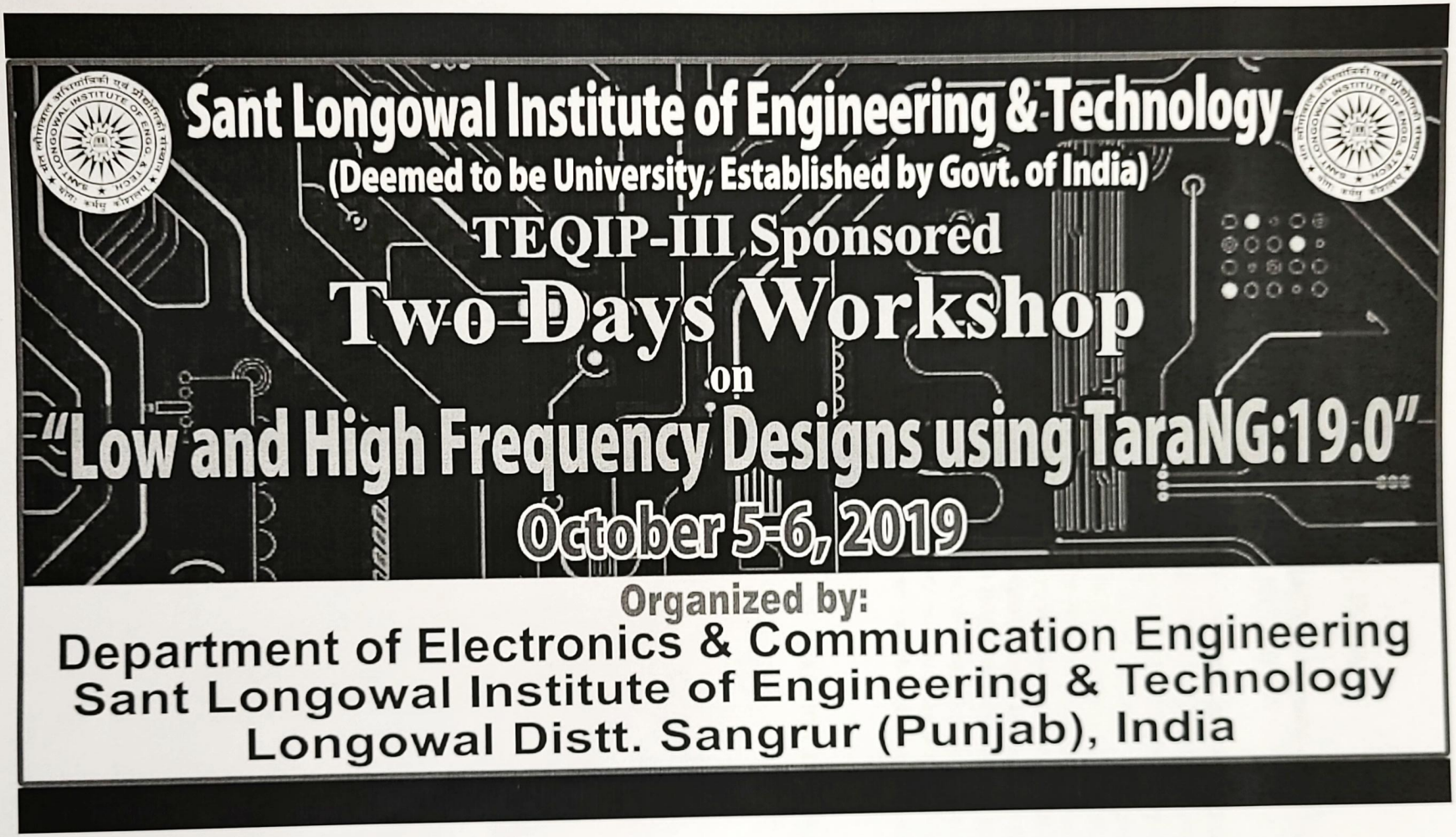
Hands on sessions on virtual lab for postgraduate and undergraduate students were scheduled on 13th and 14th February, respectively.

Resource Person:

1. **Er. Swapnil Narhari Gaul:** Founder and Director | NUMEREGION, Delhi NCR
2. **Madhura Barshikar :** Application Engineer | NUMEREGION, Delhi NCR

Coordinators:

1. **Dr. A Marwaha (Professor, ECE)**
2. **Kuldip Singh (AP, ECE)**


Sant Longowal Institute of Engineering & Technology
(Deemed to be University, Established by Govt. of India)
TEQIP-III Sponsored
Two-Days Workshop
on
"Low and High Frequency Designs using TaraNG:19.0"
October 5-6, 2019
Organized by:
Department of Electronics & Communication Engineering
Sant Longowal Institute of Engineering & Technology
Longowal Distt. Sangrur (Punjab), India

Workshop Report

"Low Frequency (LF) and High Frequency Design (HF) Using TaraNG:19.0"

Two-day workshop on, "**Low Frequency (LF) and High Frequency Design (HF) Using TaraNG:19.0"** is organized by the department of **ECE** Under **TEQIP-III** during **5th-6th October 2019** for the undergraduate students of the institute. First day of workshop covered the insight on circuit simulations i.e. **mathematical modelling** of electronics components and provided insight on how the simulation algorithms are developed. During this, hands-on session on **linear and non-linear circuits** are conducted. At the end of session **non ideal behavior** of the electronic systems and effect of parasitic are discussed. The second day of workshop demonstrated the need of 3D software for design of electronics systems and briefed on **EMI/EMC** issues, signal crosstalk and need of S Parameters analysis at higher frequency. Second day focused on **Antenna Design** with modelling and simulation of sets of antennas especially Wire Antennas. After the end of workshop, students will be able to learn how computers are solving the electronics designs and helping us in entire product life-cycle at industries. Also, students will be able to develop and code their own algorithms to solve electronics designs.

Resource Person:

Er. Swapnil Narhari Gaul: Founder and Director | NUMEREGION, Delhi NCR

Personal Details:

First Name of Applicant: Pankaj Kumar Title: Prof. Institution: Sant Longowal Institute of Engineering & Technology (SLIET, Longowal)	Surname: Das Gender: M
Applicant's Mailing Address: Er. Pankaj Kumar Das Assistant Professor Electronics & Communication Engg. Department, Sant Longowal Institute of Engg. & Tech., Longowal. Deemed University (Established by Govt. of India) District: Sangrur (Punjab) 148106, India.	Telephone: 01672-253331 Mobile (if preferred): +919478214936 Fax: 01672-253117 E-mail: Pankaj.jkd@gmail.com

Name of the Event: Two Days Online Workshop on "Nanoelectronics & VLSI"

Date: February 11th – 12th, 2021

Venue: ECE Deptt. SLIET Longowal

Number of participants: 133

Types of Participants (i.e. academia, students, communities, government, etc.): Students

a. Please describe briefly the activities conducted as part of this grant (500 words).

Two Days Online Workshop has been conducted for UG and PG Students on "Nanoelectronics & VLSI" during February 11th -12th, 2021. Following experts of Academia has been delivered the experts talk:

1. ***Dr. Praveen Prajapati***
   Associate Professor, Department of ECE, A. D. Patel Institute of Technology, Gujarat
   Topic: Basics of Design of Nano Antennas
2. ***Dr. Pankaj Kumar Pal***
   Assistant Professor Department of ECE, NIT Uttrakhand
   Topic: Basics of Nanoelectronics and VLSI Design
3. ***Er. Pankaj Kumar Das***
   Assistant Professor, Department of Electronics & Communication Engineering, SLIET Longowal
   Topic: Carbon Nanotube as Global VLSI Interconnects
4. ***Er. Swapnil Gaul,***
   Founder and Director Numergion Technology (OPC) PVT LTD, PUNE Maharashtra-411014
   Topic: Advanced simulation based virtual lab: MyTaraNG Cloud

b. Was this event successful in achieving the intended objectives and how? (300 words)
After having rigorous brainstorming, it is observed that the workshop in question was conducted meticulously for the target group including UG and PG Students with the achievement of the following aims/objectives:

- ✓ Provided broad exposure to the participants about the various aspects of Nano-electronics & VLSI design.
- ✓ Enabled the participants in the field of Electronics and Communication Engineering to introspect and learn techniques that help them for active and successful participants in a knowledge society.
- ✓ Enhanced the student's effectiveness in learning and research in the field of nano-electronics & VLSI design, modeling and simulation of device and circuits.
- ✓ Enriched the knowledge of participants by exposing them to latest trends and dimensions in nano-electronics such as spintronics, GaN and SiC devices.

Provided interaction with experts, which helps the participants to initiate their research in recent area in VLSI.

c. Enlist the possibilities wherein the event could promote SICI in your organization? (100 words)
1. We can Sign MOU for collaborative research with the Canadian Universities/School
2. Short out the possibilities to organize Conference in collaboration with SICI.
3. Will encourage the students to participate in different programme announced by SICI time-to-time.

d. Please indicate future plans (if any) based on the experience of this event.
We could conduct Five-day Short-Term Course for faculty, Research Scholar, Industry Persons and Students.

e. Please provide your feedback (if any) on the SMDG grant.
I am thankful to SICI for awarding SMDG grant to me. While organizing the workshop it seems we need more money for successful conduction of programme. So, please increase the amount of SMDG Grant.

FINANCIAL REPORT

Note: Please Complete The Following Financial Report Detailing All Your Expenses As Part Of This Grant.

Description of items (expenses)	**Amount**
Remuneration to Experts Dr. Praveen Prajapati, AD Patel Institute, Gujarat	Rs. 5000/-
Remuneration to Experts Dr. Pankaj Kumar Pal, NIT Uttarakhand	Rs. 5000/-
Remuneration to Experts Er. Pankaj Kumar Das, SLIET Longowal	Rs. 5000/-
Remuneration to Experts Er. Swapnil Gaul, Director Numergion Technology	Rs. 5000/-
Total Expenses	Rs. 20,000/-
Funds received by the Shastri Institute	Rs. 20,000/- (Rs. 17000/- as an advance. Rs. 3000/- is due)